

REMARKS

Claims 1-20 are pending. Claims 1, 2, 19, and 20 have been amended for clarity. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Objections to the Specification

The specification is objected to because of minor errors introduced during translation. Accordingly, Applicants have reviewed the specification and the claims to correct these errors. Therefore, Applicants respectfully request reconsideration and withdrawal of this objection.

Claim Rejections Under 35 U.S.C. § 112

Claims 2, 9-13 are rejected under 35 U.S.C. § 112, second paragraph. With regard to claim 2, Applicants have amended claim 2 for clarity, Applicants intended meaning. With regard to claims 9-13 applicants respectfully traverse this rejection because the recitation of “supplying a controlled quantity....” satisfies the requirements of 35 U.S.C. § 112, second paragraph. Patentability of a method claim is not determined by the structure recited in that claim, but rather is determined by the method operations recited therein. Therefore, it is not necessary that claim 9, for example, recite a mass flow controller, however the recitation of the mass flow controller does not render the claim indefinite. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claim Rejections Under 35 U.S.C. § 103

A. Claims 1-4 were rejected under 35 U.S.C. § 103(a) over DeBoer et al.(U.S. Patent No. 5,910,880). Applicants respectfully traverse this rejection.

Claim 1 recites in part, a method of fabricating a capacitor comprising forming a first amorphous TaON thin film on a lower electrode. In contrast, DeBoer teaches forming a nitride layer 36 on a first capacitor plate 34 and forming a Ta₂O₅ layer on the nitride layer, which is not the same as forming a TaON thin film on the lower electrode. Therefore, DeBoer does not teach or suggest that an amorphous TaON thin film is formed on the lower electrode as recited in claim 1.

Claims 2-4 are allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence from claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

B. Claims 5-20 were rejected under 35 U.S.C. § 103(a) over DeBoer in view of Yang et al. (U.S. Patent No. 5,956,594). Applicants respectfully traverse this rejection.

Claims 5-18 are allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence from claim 1. Additionally, claims 19 and 20 recite forming an amorphous TaON thin film on the lower electrode as recited in claim 1. Since neither DeBoer (as established above) or Yang teach forming the TaON layer on the lower electrode, no combination of these two references teaches or suggests forming a TaON thin film on the lower electrode. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

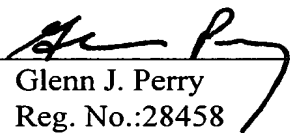
Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **“Version with markings to show changes made”**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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Enclosure: Appendix

Abstract of the Disclosure

APPENDIXVERSION WITH MARKINGS TO SHOW CHANGES MADEIN THE SPECIFICATION:

The paragraph beginning on page 1, line 22 and ending on page 2, line 3 has been replaced with the following new paragraph:

Accordingly, various methods of ensuring sufficient capacitance for DRAM capacitors have been proposed. For example, methods of increasing the area of a capacitor by modifying the physical structure of the capacitor to [from] form a three-dimensional structure such as a cylinder or reducing the thickness of a dielectric film have been used until recently.

The paragraph beginning on page 2, line 4 has been replaced with the following new paragraph:

Recently, research has also been [made] conducted to provide a dielectric film having a NO (Nitride-Oxide) structure or an ONO (Oxide-Nitride-Oxide) structure in place of the conventional silicon oxide. Other alternative dielectric films that have been considered include Ta₂O₅ or BST (BaSrTiO₃) that ensure a high capacitance providing an increased dielectric constant (typically 20 to 25).

The paragraph beginning on page 3, line 6 has been replaced with the following new paragraph:

Although the impurities existing in the Ta₂O₅ thin film may be removed by conducting a low-temperature heat treatment two or three times, (for example, a plasma N₂O or UV-O₃ treatment) these processes can be complex and their results unreliable. Furthermore, these processes have a drawback in that they will induce oxidation of the lower electrode at its interface with the Ta₂O₅ thin film.

The paragraph beginning on page 6, line 6 has been replaced with the following new paragraph:

Fig. 5 is a schematic view illustrating a procedure for removing oxygen vacancies and carbon compounds by conducting an annealing process for a deposited TaON thin film of a multi-layer structure in accordance with the method of the present invention.

The paragraph beginning on page 7, line 1 has been replaced with the following new paragraph:

In order to connect each capacitor to an associated one [in] of the active regions of the silicon substrate 10, the interlayer insulating film 20 is then selectively removed in accordance with conventional photolithography and etch processes, to form contact holes (not shown).

The paragraph beginning on page 7, line 23 and ending on page 2, line 2 has been replaced with the following new paragraph:

Furthermore, nothing in the present invention [presents] prevents the lower electrodes from having a structure that is a simple stack shape or more complex structure such as a cylinder shape, a fin shape, and a stack cylinder shape.

The paragraph beginning on page 9, line 18 and ending on page 10, line 4 has been replaced with the following new paragraph:

Another technique[s] for preventing the formation of a non-uniform natural oxide film on the lower electrodes and thereby prevent the subsequent generation of leakage current at the lower electrodes, involves feeding the wafer into a low-pressure chemical vapor deposition (LPCVD) chamber under a low pressure of typically less than 10 torr, and subjecting the wafer to an oxidation process using plasma in an in-situ H₂O atmosphere to homogeneously oxidize the surface of the lower electrodes, to form an exceedingly thin but uniform oxide film (not shown) having a thickness of 10 Å or less.

The paragraph beginning on page 13, line 10 has been replaced with the following new paragraph:

After the second TaON thin film 32b is deposited over the first TaON thin film 32a, it is subjected under a N₂O or NH₃ atmosphere [an NH₃ or], to an annealing process in an electric furnace for 5 to 60 minutes or to a rapid thermal process for 1 to 10 minutes. In accordance with this procedure, and as was the case with the first TaON thin film 32a, volatile carbon compounds and H₂O in the second amorphous TaON thin film 32b are completely removed. Similarly, the second TaON thin film is induced to crystallize, thereby avoiding a generation of leakage current.

The paragraph beginning on page 14, line 1 has been replaced with the following new paragraph:

Further, the deposition of the amorphous TaON thin films and the subsequent annealing of those deposited layers serve to eliminate structural defects, such as micro cracks and pin holes, at interfaces while producing a homogenous dielectric thin film [finally produced].

The paragraph beginning on page 14, line 6 has been replaced with the following new paragraph:

As is apparent from the above description, the methods for fabricating capacitors for semiconductor devices in accordance with the present invention provide various effects.

The paragraph beginning on page 15, line 3 has been replaced with the following new paragraph:

That is, in accordance with the present invention, it is possible to control and establish [and] the equivalent oxide film thickness for the TaON dielectric film of 25 Å or less, as compared to conventional Ta₂O₅ dielectric films in a metal-insulator-silicon (MIS) structure. This makes it possible to obtain the high levels of capacitance required for the operation of DRAMs of [256 M] grade 256 MB and higher.

The paragraph beginning on page 15, line 10 has been replaced with the following new paragraph:

In accordance with the present invention, the formation of the dielectric film is achieved by depositing a TaON thin film and treating the deposited film with a plasma process in an in-situ fashion in a LPCVD chamber. Accordingly, it is possible to eliminate the rapid thermal process conventionally conducted in a nitrogen atmosphere just prior to the deposition of conventional dielectric films. Further, it is possible to eliminate low-temperature and high-temperature thermal treatments typically conducted after the deposition of conventional dielectric films.

The paragraph beginning on page 15, line 20 and ending on page 16, line 2 has been replaced with the following new paragraph:

With the improved dielectric constant, the present invention can reduce the number of unit processing steps used and the processing time [in] by rendering it unnecessary to use any process steps for increasing the surface area of lower electrodes to obtain a high dielectric constant. Accordingly, it is possible to reduce the manufacturing costs while improving productivity.

IN THE CLAIMS:

Claims 1, 2, 19, and 20 have been amended as follows:

1. (Amended) A method for fabricating a capacitor of a semiconductor device, the method comprising [the steps of]:
 - forming a lower electrode on a semiconductor substrate;
 - forming a dielectric layer on the lower electrode by
 - forming a first amorphous TaON thin film on the lower electrode;
 - annealing the first amorphous TaON thin film in an NH₃ atmosphere;
 - forming a second amorphous TaON thin film on the lower electrode; and
 - annealing the second amorphous TaON thin film to form a multilayer TaON dielectric film; and
 - forming an upper electrode over the TaON dielectric film.

2. (Amended) The method according to claim 1, wherein forming the lower electrode further comprises one of: [forming a structure selected from a group consisting of]
 - 1) forming a single conductive layer, the single conductive layer being formed from [a] at least one material selected from a group consisting of doped polysilicon and metal, and
 - 2) forming a plurality of conductive layers, the plurality of conductive layers comprising at least two layers, the plurality of conductive layers being formed from at least one [or more] material[s] selected from a group consisting of doped polysilicon and metal; and

further wherein forming the upper electrode further comprises one of: [forming a structure selected from a group consisting of]

 - 1) forming a single conductive layer, the single conductive layer being formed from [a] at least one material selected from a group consisting of doped polysilicon and metal, and

2) forming a plurality of conductive layers, the plurality of conductive layers comprising at least two layers, the plurality of conductive layers being formed from at least one [or more] material[s] selected from a group consisting of doped polysilicon and metal.

19. (Amended) A method for fabricating capacitors for semiconductor devices, comprising [the steps of]:

- forming a lower electrode on a semiconductor substrate;
- forming a first amorphous TaON thin film over the lower electrode;
- annealing the first amorphous TaON thin film in an NH₃ atmosphere;
- forming a second amorphous TaON thin film;
- annealing the second amorphous TaON thin film a first time;
- annealing the second amorphous TaON thin film a second time, thereby forming a TaON dielectric film having a multi-layer structure; and
- forming an upper electrode over the TaON dielectric film.

20. (Amended) A method for fabricating capacitors for semiconductor devices, comprising [the steps of]:

- forming a lower electrode on a semiconductor substrate;
- nitriding an upper surface of the lower electrode in an NH₃ atmosphere;
- forming a first amorphous TaON thin film over the lower electrode;
- annealing the first amorphous TaON thin film in an NH₃ atmosphere;
- forming a second amorphous TaON thin film;
- annealing the second amorphous TaON thin film at least once, thereby forming a TaON dielectric film having a multi-layer structure; and
- forming an upper electrode over the TaON dielectric film.

IN THE ABSTRACT OF THE DISCLOSURE:

The abstract has been amended as follows:

Disclosed is a method for fabricating capacitors for semiconductor devices. This method includes the steps of forming a lower electrode on an understructure of a semiconductor substrate, depositing an amorphous TaON thin film over the lower electrode, annealing the deposited amorphous TaON thin film in an NH₃ atmosphere, and repeating the

deposition of the amorphous TaON thin film and the annealing of the deposited amorphous TaON thin film at least one time, thereby forming a TaON dielectric film having a multi-layer structure, and forming an upper electrode over the TaON dielectric film. The TaON dielectric film having a multi-layer structure exhibits a dielectric constant that is superior to those of conventional dielectric films. Accordingly, the TaON dielectric film of the invention can be used for capacitors in next generation semiconductor memory devices of [256 M grade] grade 256MB and higher.

End of Appendix

ABSTRACT OF THE DISCLOSURE

Disclosed is a method for fabricating capacitors for semiconductor devices. This method includes the steps of forming a lower electrode on an understructure of a semiconductor substrate, depositing an amorphous TaON thin film over the lower electrode, annealing the deposited amorphous TaON thin film in an NH_3 atmosphere, and repeating the deposition of the amorphous TaON thin film and the annealing of the deposited amorphous TaON thin film at least one time, thereby forming a TaON dielectric film having a multi-layer structure, and forming an upper electrode over the TaON dielectric film. The TaON dielectric film having a multi-layer structure exhibits a dielectric constant that is superior to those of conventional dielectric films. Accordingly, the TaON dielectric film of the invention can be used for capacitors in next generation semiconductor memory devices of grade 256MB and higher.